A Survey of Circuit Level Techniques for Designing Ultra Low Power, Low Frequency OTA

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Abstract- **With the advent of portable and implantable gadgets especially in biomedical field, low power analog circuit design is gaining utmost importance now a days. The study of various circuit level low power techniques like Bulk Driven (BD), Source Degeneration (SD), and class AB configuration is carried out. The advantages and the disadvantages of each of these techniques have been discussed along with the tabulation of the technology used and the power dissipation in each technique.**

Keywords - OTA, Miller OTA, Source Degeneration, Bulk Driven, Class AB configuration.

I. INTRODUCTION

Continuous shrinking of dimensions in VLSI technologies along with the growing trend of portable devices led to the necessity of power reduction from the past decade. The strong motivation behind this power reduction are such as (1) portable equipment capable of the operating with minimum number or size of battery cells to reduce volume and weight (2) longer operating periods without battery recharging or replacement (3) voltage limitations resulted from smaller feature sizes of modern IC technology.

The OTA is a basic building block in analog circuit applications including continuous-time filters, data converters, variable gain amplifiers and other interface circuits. Due to scaling down of device sizes, supply voltage and power consumption to achieve higher operating speeds, obtaining high linearity becomes ever challenging. Several circuit techniques have been proposed and they include: Source Degeneration, Bulk Driven, Class AB configuration, Bulk Degeneration, cross-coupling of multiple differential pairs, Adaptive Biasing and series connection of multiple differential pairs. This survey paper compares and analyses these low power techniques both qualitatively and quantitatively. In sections II, III and IV, the non-conventional techniques based on source degeneration, bulk driven and class AB configurations have been presented along with the main advantages and drawbacks of each technique. Finally section V concludes the paper.

II. SOURCE DEGENERATION TECHNIQUE

This is one of the techniques used to reduce power consumption and to increase linearity of OTA. In the case of simple resistor implementation of source degeneration, then a very large resistor must be used which consumes large power and chip area. Instead of a resistor if two MOS transistors operating in triode region are used, then power and chip area requirement reduces but non-linearity will be present up to 1% for I_{out}/I_{ss}. In the case of a simple class AB linearity technique, non-linearity will occur below the supply voltage of 2V. So Trung-Kien Nguyen and Sang-Guglee [1] proposed operational transconductance amplifier which is the combination of source degeneration using MOS transistor and class AB linearization technique which is based on standard 0.25µ CMOS technology with supply voltage of 1.27V and power consumption of 25µw. The total harmonic distortion (THD) is also low with 60dB at 5MHz for $0.6V_{p-p}$. This type of OTA is suitable for G_mC filter implementation. To reduce the THD, X.Zhu and Y.Sun [2] proposed another modified OTA in 2008 where the total harmonic distortion is brought down below 1% upto $0.85V_{p-p}$. As the available voltage headroom becomes limited, many existing circuit techniques in the analog domain cannot be applied. Very often large-gate source voltages are required in order to improve linearity but the supply voltage limit this. So the authors [2] use flipped voltage follower (FVF) to reduce power supply and source degeneration techniques to optimize power consumption and linearity. Here differential pair in the input stage with source degeneration is used and the output stage consists of four current mirrors. The common mode feedback (CMFB) circuit is used to stabilise DC output voltage. The OTA was simulated in the standard 0.18µm CMOS technology with 1.8V supply voltage. The power dissipation is 11.8mW and the transconductance is 1.1mS. This type of OTA is suitable for wireless communication receiver baseband applications.

To decrease the transconductance, Jun-Yen Lin, Wein-Hsin Chang and Chung-Chih Hung [3] proposed an OTA design, where the G_m value ranged from 60µS to 130µS. This OTA design combines the techniques of the double differential pairs (DDP) and source degeneration current mirror. As the

value of source degeneration resistor R increases, the value of G_m reduces; which implies low operational speed therefore, double differential pair is used to improve linearly. But in DDP, the resistor value must be tuned first, which may lead to degradation of linearity. So source degeneration current mirror is used to achieve a large G_m tuning range without degrading the circuit linearity. The advantage of source degeneration current mirror is when tuning G_m value, it only changes the bias voltage of the output pairs, and the bias voltage of the input pairs is not changed. So, linearity is maintained and common mode feedback circuit is used to stabilize the output common mode voltage. The OTA was simulated in a standard 0.18µm with1.8V power supply. The power consumption is 1.21mW. This type of OTA is suitable for G_mC filter implementation.

TABLE 1: SUMMARY OF SOURCE DEGENERATION TECHNIQUE

	Technology	**Technique**	**Power**
Nguyen and Guglee [1]	0.25µm	Source degeneration and class AB technique	25µW
X.Zhu and Y.Sun [2]	0.18µm	Source degeneration and flipped voltage follower	11.8mW
Lin, Chang and Hung [3]	0.18µm	Source degeneration and double differential pairs	1.21mW

From Table 1, it is evident that the OTA employing Source Degeneration and Double Differential Pairs technique is more power efficient than that with Source Degeneration and Flipped Voltage Follower technique. The advantage of these techniques is that they are more linear and even boosts the output impedance. Disadvantages being the smaller usable output swing, noisier due to the source resistor and increase in area because of passive elements.

III. BULK DRIVEN TECHNIQUE

In Bulk driven technology, as the input is applied to bulk terminal the body transconductance is approximately five times smaller than the gate transconductance which result in the relatively low gain. To improve the gain, Jonathan Rosenfeld, Mucahit Kozak, and Eby G. Friedman [4] in the year 2003 proposed the topology based on bulk driven which uses four common-source gain boosting amplifier. The output branch consists of common gate amplifier with cascade current loads to increase the gain and common mode feedback circuit is used with four auxiliary common source amplifiers. The rail-to-rail operation of the amplifier is also supported as pair of pMOS and nMOS transistors are used in the input stage as shown in [4]. Common source amplifier provides an open loop gain which will avoid stacking multiple transistors in the output branch and to maintain transistor in the saturation region. The output of the common source amplifier is connected to gate of the common gate amplifier so as to maintain an almost constant source voltage. The OTA was stimulated in standard 0.18µm with 0.8V power supply. The power consumption is 94µw and an open-loop DC gain of 68 dB.

Lihong Zhang, Xuguang Zhang, Ezz El-Masry and Yuping Zhang [12] proposed the topology in 2007 based on bulk driven with common mode feedback and common mode feed forward. The common mode feed forward circuit was employed to adjust the bias voltage of OTA. This was stimulated in standard 0.18µm with 1.8V power supply and the power consumption was 4.07mw.

As in the inversion region the pow consumed is less so, Shouri Chatterjee, Yannis Tsividis, and Peter Kinget [5] in the year 2005 proposed a fully differential two stage Miller operational amplifier. As the signal is applied to bulk of the device, for an input common mode at $V_{DD}/2$, a small forward bias for the bulk source junction is also introduced which lowers threshold voltage and further increase

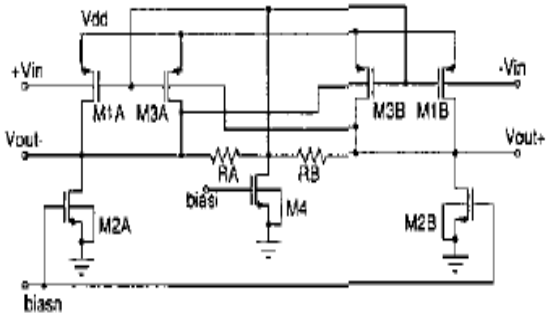

Fig.1. Fully differential single stage operational amplifier.

to operate in the inversion level. As seen in the Fig.1, the inputs are given to bulks of pMOS transistor they are loaded by the nMOS transistors which acts as current source. Resistors are used to detect the output common mode voltage which is feedback to the gates of pMOS devices. The bulk inputs of M3A and M3B form a cross coupled pair that adds a negative resistance to the output and boots the differential DC gain. By cascading two identical gain blocks, a two stage OTA is obtained [5] and Miller compensation capacitor $C_c$is added to stabilize the amplifier. The OTA was stimulated in standard 0.18µm with 0.5V

power supply. The power consumption is 110µw and DC gain is 52dB.

To decrease the power consumption in the inversion region using Miller OTA Luís H. C. Ferreira and Tales Cleber Pimenta [6] in the year 2007 proposed the OTA which works in the inversion region, as under the weak inversion region the signal swing is larger than on strong inversion due to lowV_{DS} , but the frequency response is reduce to extremely low current, if $V_{DS} \geq \frac{3kT}{q}$, then transistor will be saturated in

$$g_m = q\frac{I_{DS}}{nkT} \ldots\ldots\ldots (1)$$

weak inversion. The transconductance $g_m$can be found as presented in (1), which is a function of current I_{DS} and factor $\frac{\eta kT}{q}$ only. The transconductance $g_{mb}$is given by (2). The transconductance g_{mb}varies from 20% to 30% of g_m for

$$g_{mb} = \frac{\gamma}{2\sqrt{2\varphi_F - V_{SB}}} g_m \ldots . (2)$$

the same transistor in a CMOS process. The important configuration for MOS transistor in weak inversion is the composite transistor. The nMOS composite transistor is as shown in Fig.2.

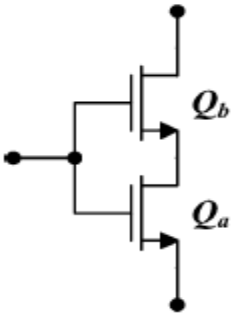

Fig.2. Composite transistor with common well

The current and voltage expression of the composite transistor is given [6] this expression is the function of the transistor sizes and the CMOS process parameter, valid for weak inversion only and it is independent of transistor gate-source voltage. The author proposed the Miller OTA where two batteries were placed in series with active load to avoid distortion to the signal [6]. The circuit was not capable of generating voltages but were capable of providing voltage drops, thus emulating batteries. So, battery is replace by common-gate amplifier as shown in Fig 3, which was known as improved Miller OTA and even the transistors were in saturation region, which gives gain. This topology was stimulated in standard 0.35µm CMOS process is capable of working with 600mV, consumes 550nw and gain is 73.5dB. The advantage is additional biasing source is not required and disadvantage is large input capacitance and low DC gain. This circuit is used in high time constant applications such as

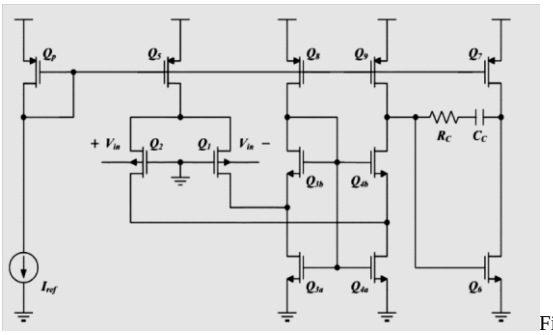

Fig.3. Improved Miller OTA circuit.

band gap, physical transducer, process controller and mainly on small battery operated devices.

To improve the DC gain in the Miller OTA Milad Razzaghpour and Abbas Golmakani [7] proposed the topology based on a bulk-driven input differential pair employed a gain-stage in the Miller capacitor feedback path. As the disadvantage of the Miller technique is the inconvenience of the right half plane (RHP) zero, which degrades the phase margin and leads to instability of operation. This can be overcome by nulling resistor control in fig 3 or by employing gain stage that prevent the input current directly going through the miller capacitor as given in [7]. So, in the proposed Miller OTA the resistor have been replaced where DC gain is independent of g_m and g_{mb}, the unity gain bandwidth is also enhanced using common gate in Miller capacitor feedback path as given in [7]. The dominant pole is same as normal Miller composite OTA but there is the need to increase the output pole. This topology was stimulated in standard 0.18µm CMOS process is capable of working with 0.5V, consumes 1.02µw and gain is 88.5dB. The advantage of this is no passive elements are used but the power consumption has been increase.

Meng-Hung Shen, Yi-Shuan Wu, Guan-Hung Ke and Po-Chiun Huang [8] proposed two stage pseudo differential amplifier in the year 2010, rail-to-rail operations is also achieved. Applying pseudo-differential structure, the input common mode range is extended. Drawback of this type of circuit is, its common mode gain is equal to the differential mode gain. This type was simulated in the standard 0.18µm with 0.7V power supply and power consumption is 107nw.

To achieve high linearity in lower power supply Apiradee Yodtean, Pasin Isarasena and Apinut Thanachayanont [9] proposed the topology in 2010 based on bulk driven differential input stage using source degeneration technique and flipped voltage follower and MOSFET are driven in subthreshold region. The Bulk driven technique is used at input stage of transconductance to allow wide range linear input, DC input common mode voltage to be in the middle of supply and a larger input voltage range at the cost of

lower transconductance. Linearity can be improved by using resistive source degeneration, gate degeneration, bump linearization and parallel connection of input differential pair. This technique is simulated using standard 0.35µm technology with 0.8 supply voltage. The power consumption is 0.8µw. It is basically designed for Biomedical and neural network ic's and systems.
Yen-Ting Liu, Donald Y.C.Lie, Weibo Hu, Tam Nguyen[10] proposed the topology in 2012 based on bulk driven and source degeneration and the transistor are driven in weak inversion region, the power consumption was very less compared to subthreshold i.e 750nw at 3V supply voltage and the technology used is 0.35µm.

The Dynamic threshold MOS technique using bulk and gate driven input differential pair was proposed by Ehsan Kargaran, Mohamad Sawan, Kalil Mafinezhad, Hooman Nabovati [11] which employs a gain stage in Miller capacitor feedback path to improve pole splitting effect. In DTMOS the gate and body are tied together so it reduces leakage current in OFF state and reduces threshold voltage during ON state to increase overdrive voltage .The transistors are driven in weak inversion and are simulated in standard 0.18µm technology with 0.4V power supply and power consumption is 386nw. This technique can be used in biomedical field.

To achieve high linearity and to suppress the common mode signals Tomasz Kulej [13] proposed the topology in 2010 based on bulk driven where Common Mode Feed Forward (CMFF) is used. Here all the transistors are operated in the moderate inversion region to achieve linearity. The overall transconductance is reduced by using long channel output transistor. The use of this long channel output transistor aids to the increase output resistance of the device and also the voltage gain of the OTA. The performance is verified by LT SPICE stimulation in 50nm CMOS technology with power supply of 0.5V, the power consumption of the proposed OTA is 107nw.

Ming-Kai Fu, Miin-Shyue Shiau, Hong-Chong Wu, Don-Gey Liu [16] proposed the OTA with Common-Mode Feed-Forward technique . This method replaces the (CMFB and Cascode current mirror technique) conquering operation of the common mode signal and noise at the input nodes by feeding them inversely through another path forward to the output mode, then the common mode small signal which come from both paths would be cancelled at output node by superposition-addition. The Technology employed is the standard 0.35µm with power supply of 1.1V having a power dissipation of 63µW.
The three techniques were merged to obtain low power, low voltage and wide linear range operation by Surachoke Thanapitak in the year 2013. The techniques are bulk driven , drain current normalisation and floating gate. Using these techniques implemented OTA is as shown in [19]. This was stimulated in standard 0.18µm with 1V supply voltage and power consumption was 48.98nw.

The advantage of this technique is that it has depletion characteristic that dissolve the threshold voltage requirement of the conventional MOS transistor, it has the wide dynamic bias range as the signal is directly applied to the bulk terminal and the disadvantage is that the $g_m$is smaller than that of a conventional gate driven MOS transistor, which may result in low and worse frequency response. It is even the more expensive process as the dual well process is needed.

TABLE 2: SUMMARY OF BULK DRIVEN TECHNOLOGY

	Technology	**Technique**	**Power Consumption**
Rosenfeld, Kozak, and Friedman[4]	0.18µm	Bulk driven	94µw
Zhang, Xuguang Zhang, Masry and Zhang [12]	0.18µm	Bulk driven with CMFF and CMFB	4.07mw
Chatterjee, Tsividis, and Peter Kinget [5]	0.18µm	Bulk driven with Miller OTA	110µw
Ferreira and Pimenta [6]	0.35µm	Bulk driven with Miller OTA	550nw
Razzaghpour and Golmakani [7]	0.18µm	Bulk driven with Miller OTA	1.02µw
Shen, Wu, Guan-Hung and Huang [8]	0.18µm	Bulk driven in pseudo-differential OTA	107nw
Yodtean, Isarasena And Thanachayanont [9]	0.35µm	Bulk driven, source degeneration and flipped voltage follower	0.8µw
Liu, Donald Y.C.Lie, Hu, Tam Nguyen [10]	0.35µm	bulk driven and source degeneration	750nw
Kargaran, Sawan, Mafinezhad, Nabovati [11]	0.18µm	bulk driven with DTMOS	386nw
Tomasz Kulej [13]	50nm	bulk driven with CMFF	107nw
Kai Fu, Shiau, Chong Wu, Don-Gey Liu[16]	0.35µm	bulk driven with CMFF	63µw
Surachoke Thanapitak[19]	0.18µm	Bulk driven and floating gate MOSFET	48.98nw

IV. CLASS AB TECHNIQUE

Hybrid Class A/AB is the one that combines a folded cascode as the first stage with active current mirror in the second stage. Mohammad Yavari and Omid Shoaei [14] proposed a two stage OTA that has a Class A/AB structure with new hybrid cascode compensation scheme that enhances its speed, the Class AB structure reduces the power consumption of OTA. The OTA has been designed for a switched capacitor integrator where sampling, integrating and load capacitance was 2.5pF, 10pF, 2pF. The merged cascade compensation technique used results in fast settling compared to conventional Miller technique but the proposed methodology has the more complex design procedure. It was stimulated using 0.25µm technology in HSPICE and the power consumption is 8.9mw. The conventional Class AB has following disadvantage such as: large chip area, limited voltage operation and limited input common mode range. The class AB OTA with negative resistance Airong Liu, Huazhong Yang [17] proposed the rail-to-rail. The architecture of rail-to-rail OTA is based on current mirror topology with feedback between the output nodes of the first stage as shown in [17]. The current mirror is used to obtain low power and rail-to-rail output swing. The negative resistance is used for compensating parasitic resistance. The OTA was proposed in 2007 and it has been stimulated in the 0.18µm technology with 1V power supply and power consumped is 67µw.

Ah-Reum Kim, Hyoung-Rae Kim, Yoon-Kyung Choi, Yoon-Suk Park and Bai-Sun Kong [15] has proposed in 2009 Class AB input stage using novel adaptive biasing. Adaptive biasing circuit is used to low and control quiescent current and also temporarily increase the output current. The proposed Class AB has following stages: Class A at the input stage and Class AB at the output stage which includes novel adaptive biasing circuit which senses the voltage difference of the input and boosts the tail current. The proposed OTA has been stimulated in the standard in 0.19µm with 1.8V power supply and power consumption is 1.96µw.

The low circuit complexity OTA was proposed by Ebrahim Farshidi [18] in the year 2009 which also has adjustable voltage supply and power. The circuit consist of floating gate MOS transistors operating in saturated strong inversion. The circuit performs the linear transconductance. The OTA was proposed in the year 2009 and it has been stimulated in the standard 0.18µm with 0.7V power supply and power consumption is less than 10µw.

The advantage of this technique is that it is having good efficiency, low distortion and it will produce broad bandwidth but the disadvantage is that it has limited dynamic range.

TABLE 3: SUMMARY OF CLASS AB CONFIGURATION.

	Technology	**Technique**	**Power**
Yavari and Shoaei[14]	0.25µm	Class AB	8.9mw
Airong Liu, Huazhong Yang [17]	0.18µm	Class AB	67µw
Kim, Choi, Park and Kong [15]	0.19µm	Class AB	1.96µw.
Ebrahim Farshidi [18]	0.18µm	Class AB	10µw

V. CONCLUSION

Different circuit level techniques used to minimize the power consumption in designing the Operational Transconductance Amplifier (OTA) are discussed and the power consumption in each technique has been tabulated. Each technique has its own advantages and disadvantages and depending upon the applications the suitable techniques may be employed.

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